Secondary Electron Imaging of Nucleation and Growth of Semiconductors

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(Received: Jan. 31, 1997 Accepted: Feb. 20, 1997)

Abstract

We have used *in situ* scanning electron microscopy (SEM) for real-time observation of the epitaxial growth processes of semiconductor surfaces. In solid phase epitaxy of Ge on Si(111), Ge island formation initially occurs at steps and out-of-phase boundaries of (7×7) domains. A monolayer of As overlayer deposited on the amorphous Ge layer raises the Ge crystallization temperature by up to 100°C both on 7×7 and "1×1" regions on the Si(111) substrate, as well as suppresses islanding of Ge. For GaAs epitaxy, the surface morphologies are compared between molecular beam epitaxy (MBE) and migration enhanced epitaxy (MEE). Surface roughness during MEE growth is about one monolayer and much smaller than during MBE growth. Immediately after growth termination, monolayer steps can be seen and the surface recovers to initial smoothness in MEE, while islands do not disappear without higher temperature annealing in MBE.

1. Introduction

An observation technique that offers atomic layer sensitivity together with nanometer-scale lateral resolution is useful for *in situ* characterization of nanostructure fabrication on semiconductor surfaces. We have shown that scanning electron microscopy (SEM) in ultrahigh vacuum (UHV) can image surface atomic layers, such as reconstructed surface domains [1] and nucleating 2D-islands [2], and that it enables dynamic characterization of growth processes [2, 3]. Secondary electron (SE) images of 2D-island nucleation and coalescence clearly showed the layer-by-layer growth in real space, and were correlated with the reflection high-energy electron diffraction (RHEED) intensity [2]. The advantages of in situ SEM are that it can image a wide range of phenomena and can monitor growth processes without growth interruptions, both of which are generally difficult for scanning tunneling microscopy (STM).

In this paper, we discuss epitaxy of semiconductors in relation to in situ imaging of nanostructure and atomically flat surface fabrications by using UHV-SEM. To investigate the effect of surface reconstruction, we observe solid phase epitaxy (SPE) of Ge on Si(111). We compare the morphologies of GaAs(001) surfaces grown by molecular beam epitaxy (MBE) and migration enhanced epitaxy (MEE) at 500°C.

2. Experimental Procedure

In situ observations were performed using the UHV-SEM/MBE system [4]. The instrument is equipped with a field emission electron gun mounted on top of the sample chamber, in which germanium, gallium and arsenic effusion cells are installed. The electron beam energy was 25 keV, with a beam current of 0.1-0.3 nA. For SEM imaging, the sample stage was tilted 60-75° from the horizontal sample position, and the electron beam was directed downward to the surface at a glancing angle of 15-30°. The scanning rate for SEM imaging was 80 seconds per frame with an effective imaging time of 73 s.

As a Si substrate, a (111) wafer (B-doped, 5 Ωcm) misoriented by 0.2° was used. A clean Si(111) surface was obtained by heating the sample resistively up to 1220°C in the sample chamber. As a GaAs substrate, a (001) wafer misoriented 0.2° toward the (110) plane, was mounted using indium soldering on a silicon substrate. The GaAs sample was heated by resistively heating the silicon substrate with direct current.

3. Ge SPE on Si(111)

Ge is known to show Stranski-Krastanov islanding on Si for above 4 monolayers of Ge [5]. Mesh pattern formation during Ge islanding has been reported for SPE of a thin amorphous Ge layer deposited on a Si(111) surface, and it was speculated that this mesh pattern is caused by preferential crystallization

of amorphous Ge at steps and at out-of-phase boundaries (OPBs) of (7×7) structures [6]. This finding is interesting from a practical viewpoint; it suggests the possibility of controlling island growth by using steps and OPBs [7].

We applied in situ SEM to the observation of Ge-SPE [8]. The Si(111) surface was transformed to step-bunched by dc resistive heating at 1220°C with a step-down current to make SEM observation easier by obtaining wider terraces. Figure 1(a) shows an SE image of a clean Si surface observed at 8°C below the (7×7) - (1×1) transition temperature (Tc). A SiC particle on the surface was used as a landmark. (7×7) regions appear brighter than (1×1) regions in the SE image [1]. Near Tc, (1×1) regions appear at steps and OPBs. Therefore, (7×7) domains are clearly imaged by SEs. There are several step bands, which are pinned by the SiC particle. Monolayer steps exist

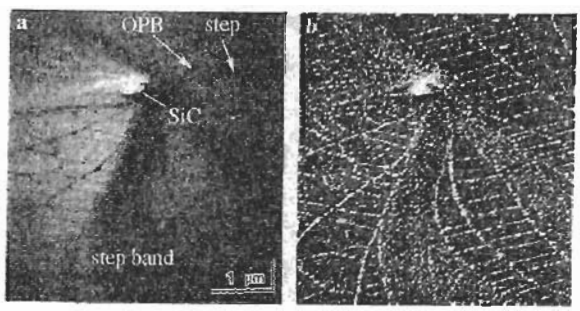

Fig. 1 SE images of SPE-Ge on Si(111). (a) Initial Si(111) surface observed near the (7×7) - (1×1) transition temperature, and (b) a 1-nm Ge deposited surface annealed at 400°C.

between the step bands. The dark lines normal to steps are OPBs of (7×7) domains. The shapes of the OPBs changed during annealing at Tc-8°C, resulting in the ladder-like structure [9].

A Ge layer 1-nm thick was deposited on the surface without heating (< 100°C). Figure 1(b) shows SE image of the surface annealed at 400°C for the same position as in Fig. 1(a). Step and OPB patterns identical to those in Fig. 1(a) are clearly seen in the micrograph. They are due to small Ge islands being nucleated at steps and OPBs.

Preferential nucleation of Ge islands at steps and OPBs was also observed for a thicker Ge layer in the initial stage of Ge island nucleation [8]. At 200°C Ge islands exist only on steps and OPBs. With increasing temperature, nucleation begins to take place even on the terraces. These observations confirm the previous speculation that Ge crystallization is initiated at steps and OPBs, causing the mesh patterns. The preference in crystallization at steps and OPBs was explained by the rigidness of the (7×7) structure [6, 7]. The (7×7) structure has been shown to be preserved upon deposition of amorphous Ge [10]. In SPE, Ge atoms have to destroy the (7×7) structure in order to be incorporated into Si lattice sites. In contrast, at steps and OPBs, which are defects of the (7×7) structure, Ge atoms do not need the extra energy for destroying the structure when they are incorporated in the lattice sites. Preferential crystallization, therefore, takes place at steps and OPBs at lower temperature.

4. Surfactant Effect on Ge SPE

Surfactants were found to alter the growth mode in SPE of Ge on Si [11-13], as well as in MBE [14]. A monolayer of Sb on the Si substrate prevented islanding of Ge during SPE [11]. Moreover, Sb [12] or boron [13] deposited on top of an amorphous Ge layer has been shown to prevent Ge islanding during SPE, although boron at the Ge/Si interface had no effect as a surfactant [13]. On the other hand, surface reconstruction affects the islanding temperatures of Ge on Si(111) surfaces in SPE, as shown in the previous section. Thus, the effect of the surfactants on the crystalline temperature is intriguing, because the surfactants are considered to affect surface binding states, while the substrate surface reconstruction affects crystallization at the interface. In contrast to MBE, where deposited surfactants inevitably affect the reconstruction on the substrate, SPE can preserve the interface reconstruction when the surfactants are deposited on top of amorphous Ge layers.

We compare the temperatures of crystallization on an As-terminated surface and an As-free surface, and on (7×7) and "1×1" regions. As-termination was done on an amorphous Ge layer by exposing the surface to the As_4 flux. Then, the SPE process was monitored by SE imaging. The results are shown in Fig. 2. Image (a) is the starting Si(111) surface prepared by quenching. (7×7) regions near steps appear brighter than "1×1" regions near the middle of wider terraces in the SE image. Image (b) shows the As-terminated amorphous Ge surface. The contrast between

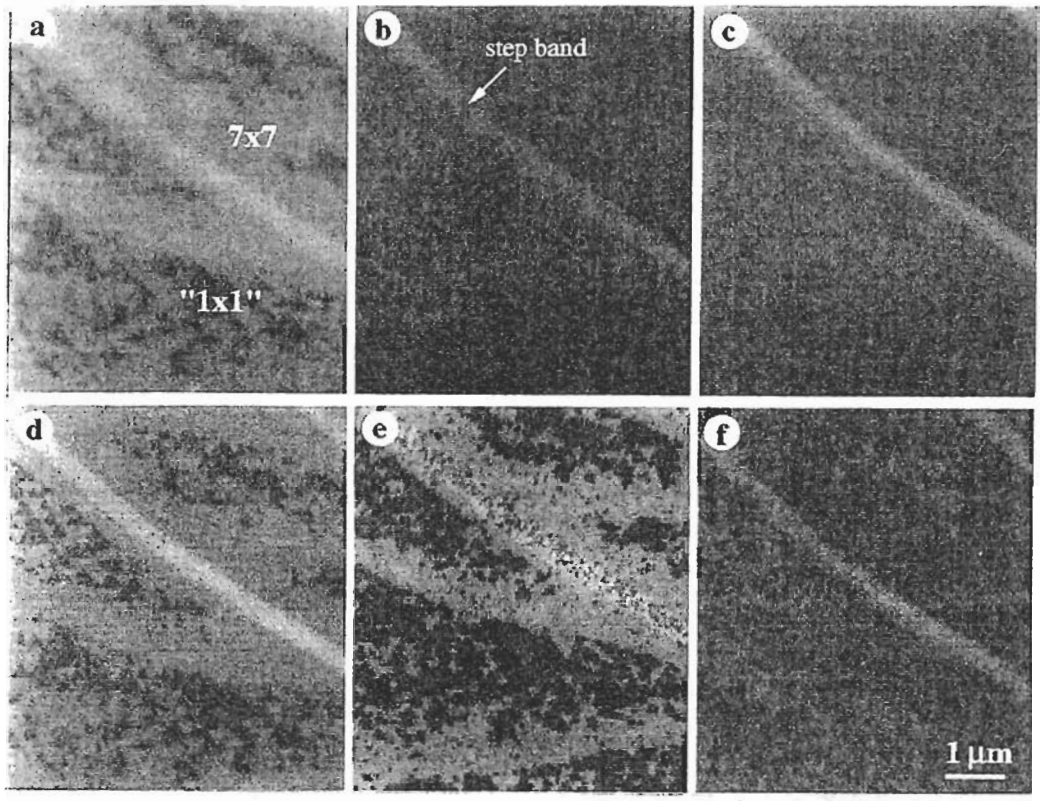

Fig. 2 SE images of As-terminated SPE-Ge on Si(111). (a) Quenched Si(111) surface before deposition, (b) a 10-nm Ge deposited surface before annealing, and after annealing at (c) 290°C, (d) 300°C, (e) 330°C, and (f) 350°C.

(7×7) regions and "1×1" regions that was seen in image (a) disappeared after the 10-nm Ge deposition. No contrast change can be seen in image (c), which was taken at 290°C. At about 300°C, a contrast similar to the starting surface appears as shown in image (d). The darker regions correspond to the initially "1×1" regions. As the temperature was increased, the darker region expanded [image (e)] and finally covered the whole surface at about 350°C [image (f)]. There still remains the pattern reflecting the starting surface structure in image (f), but it has almost disappeared at about 400°C. No islanding occurred up to 500°C.

The change in SE contrast in image (d) is due to partial crystallization of the Ge layer in the "1×1" region. This was confirmed by plan-view transmission electron microscopy (TEM) observation [15].

The above results show that an As monolayer on top of an amorphous Ge layer changes not only the growth mode, but also the crystallization temperature. A temperature almost 100°C higher is necessary to initiate SPE when an As monolayer is deposited. Furthermore, a temperature of even 50-60°C higher is necessary to crystallize Ge on the (7×7) structure compared to on the "1×1" structures. This means that the (7×7) structure is preserved up to a temperature 100°C higher than in the case of without As overlayer. Thus, the As overlayer suppresses Si and Ge atom interdiffusion at the interface.

We attribute this phenomenon to pinning of the amorphous Ge surface by As. In general, the structural relaxation of amorphous materials takes place by densification and lattice relaxation in the course of crystallization. This means that an as-deposited amorphous layer contains much excess volume and it is decreased by annealing. Some excess volume vanishes at the surface, and a surface pining effect can inhibit the roll of sink. When As passivates on top of the 10-nm amorphous Ge layer, surface diffusion is hindered, so some excess volume in the amorphous layer cannot vanish at the surface. A higher activation energy is required for the movement of the excess volume. We speculate that this is why the As passivated amorphous Ge film did not start epitaxy until a temperature 100°C higher than in the case of without As overlayer.

5. Surface Morphology in GaAs Growth

In MEE, the surface migration of Group III elements is enhanced by the alternate supply of

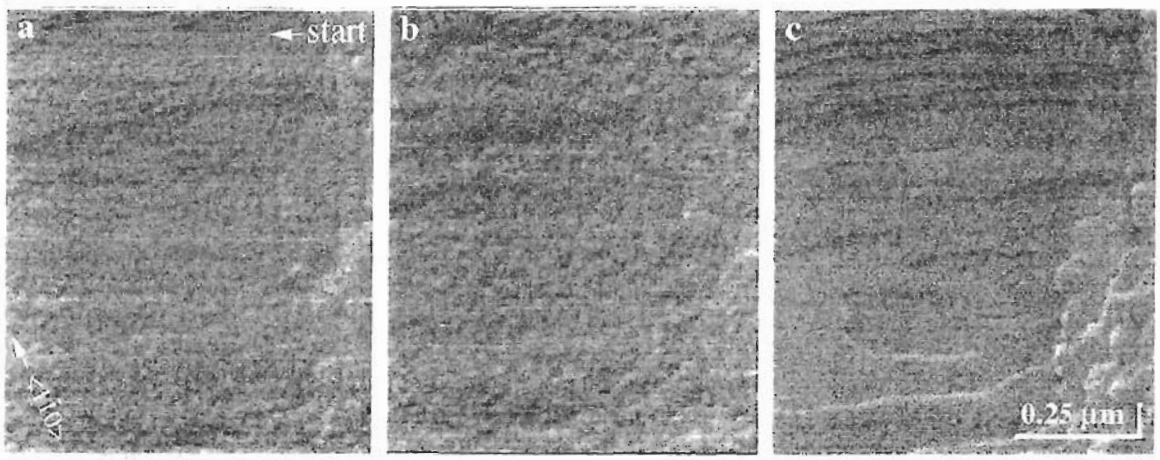

Fig. 3 SE images of MBE-grown GaAs (001) surface. (a, b) During growth at 580°C, and (c) 5-min annealed surface at 580°C after MBE.

Group III and Group V elements. As a result, a high-quality epitaxial layer can be grown at temperatures far below the MBE growth temperature range [16, 17].

We performed a comparative experiment between MBE and MEE to examine the surface migration as real-space images [3]. The observation was done at 500°C after a buffer layer of GaAs was grown by MBE at 580°C. In MEE mode growth, the Ga and As shutters were opened alternately, while they were kept open during MBE growth. The As_4 pressure was about 1×10^{-5} Torr when the As shutter was open.

In the 2D-island nucleation mode of MBE, surface roughness develops during growth, because the nucleation-coalescence cycle does not occur in an ideal manner but in an out-of-phase one, so several levels of layers coexist [18]. Figure 3 shows the surface morphology during MBE growth and after annealing at 580°C. Growth of 4-6 GaAs layers was imaged in one micrograph frame during growth. It should be noted that time-dependent morphology variations were superimposed on a normal SEM micrograph when the surface was imaged during growth or annealing. At 580°C, which is a normal temperature for MBE, the surface morphology oscillates clearly in the first three cycles as a result of nucleation and coalescence of 2D islands [image (a)]. However, the surface becomes rough due to accumulation of islands and holes in the following cycles [image (b)]. The step and terrace structure on the initial surface is buried in these multilayered islands. Nevertheless, the roughened surface easily recovers its initial smoothness after post-growth annealing. Image (c) is a 5-min annealed surface after growth termination. Steps consisting of one GaAs layer (monolayer) can be seen. Islands and holes developed during growth are incorporated into these steps and disappear.

Thus, an atomically smooth surface is hard to grow without post-growth annealing when the 2D-island nucleation growth mode occurs in MBE. In the step propagation growth mode (so called step-flow mode), a well defined step-terrace structure can be obtained during growth, but it requires a high substrate temperature or a low growth rate.

In contrast to MBE, a fairly smooth surface can be obtained even at a low substrate temperature of 500°C in MEE. In Fig. 4, the surface morphologies are compared among the initial surface (a), immediately after growth of 10 layers (b), and after annealing for 100 s (c). The initial surface shows monolayer steps, and a step bunch running from top left to middle right. During MEE growth, Ga and As were supplied alternately in amounts corresponding to 1 ML. For one cycle, the Ga shutter was opened for 11.5 s and the As shutter was opened for 3.5 s. Acquisition of image (b) started 15 s after the 10 cycles of Ga and As supply. Bright spots are islands remaining on the surface. In spite of the existence of these islands, monolayer steps almost identical to the initial surface are seen. This is because the remaining islands are only a monolayer high, and their coverage is much smaller than unity. These islands are almost annealed out in the next image (c) taken 100 s after growth termination.

In MBE, on the other hand, small Islands accumulate monotonically at 500°C. Even after

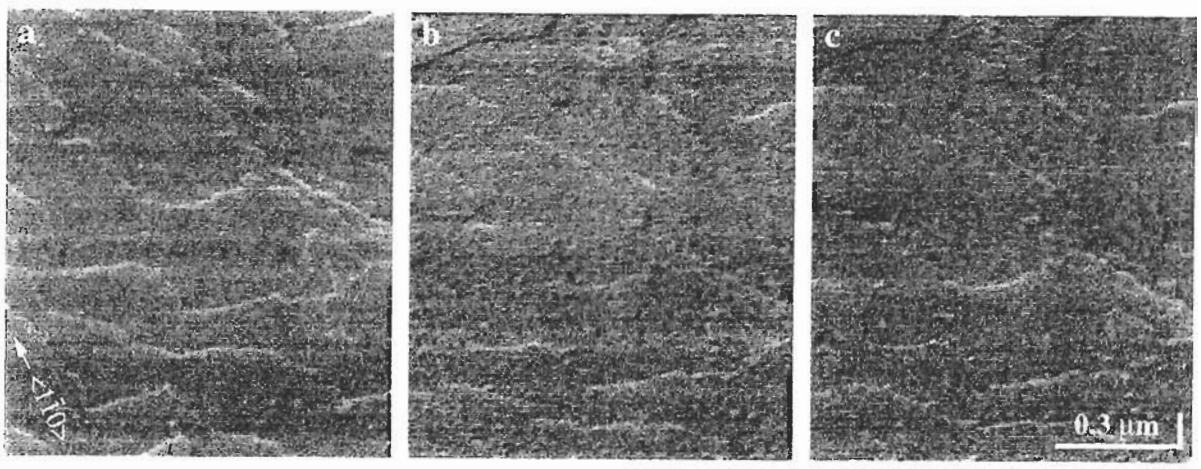

Fig. 4 SE images of MEE-grown GaAs (001) surface at 500°C. (a) Initial surface, (b) 15 s after 10-layer growth and (c) 100 s after growth.

being annealed for a long time at this temperature, the surface did not recover its initial smoothness. It was necessary to raise the substrate temperature to 550°C to anneal out these islands [3].

These results indicate that the surface diffusion is much greater in MEE than in MBE, so only monolayer-high roughness develops during growth. The surface diffusion of atoms from GaAs islands to steps during post-annealing should be the same for both MBE and MEE. The difference in recovery of surface smoothness is due to the height and density of islands. While a high density of multilayered islands are formed in MBE, Ga atoms supplied each cycle never stay on top of previously formed islands but move to edges of islands or in between them in MEE.

6. Summary

Scanning electron microscopy was used for in situ observation of epitaxial processes on Si and GaAs. Examination of solid phase epitaxial growth of Ge/Si(111) showed that Ge island formation initially occurs at the steps and out-of-phase boundaries of (7×7) domains. As overlayer deposited on an amorphous Ge layer altered the growth mode, and raised the Ge crystallization temperature by up to 100°C. Furthermore, a temperature of even 50-60°C higher is necessary to crystallize Ge on the (7×7) structure compared to on the "1×1" structures. Thus, three types of crystalline states - crystalline island, crystalline layer, and amorphous layer - can be formed on the same surface by controlling the As deposition area and the substrate temperature.

During GaAs MBE, secondary electron images clearly showed morphology change due to nucleation and growth of 2D-islands. When the surface morphology was examined at a lower substrate temperature, a smooth surface with monolayer steps was obtained immediately after MEE growth, while the surface was roughened by random nucleation in MBE growth. The present observations confirm by means of real-space images that surface migration during growth is significantly enhanced in MEE. An atomically flat surface, thus, can be grown even at a low substrate temperature in MEE.

The lateral resolution of secondary electron imaging can be improved to 1-2 nm, which is high enough to resolve most nanostructures. UHV-SEM is, thus, a promising technique for monitoring quantum structure fabrications on semiconductor surfaces.

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